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# 1 Transceiver Architecture In Stratix V Devices

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Subscribe Send Feedback For a complete understanding of Stratix® V transceivers, first review the transceiver architecture chapter, then refer to the subsequent chapters in this volume. - Mon, 22 Apr 2019 00:11:00 GMT 1. Transceiver Architecture in Stratix IV Devices - intel.com Section I. Device Datasheet and Addendum for Stratix IV ... Stratix V Device Handbook - CiteSeerX 1-2 Transceiver Architecture in Stratix V Devices 2012.12.17 Device Layout Stratix V devices have columns of transceivers on the left and right sides of the devices. Stratix V Device Handbook, Volume 3: Datasheet December 2010 Altera Corporation Stratix V Device Handbook Volume 3: Datasheet Recommended Operating Conditions This section lists the functional operation limits for the AC and DC parameters for Stratix V devices. Table 1–3 lists the steady-state voltage and current values expected from Stratix V devices. Stratix 10 GX/SX Device Overview - Mouser Electronics 1. Intel® Stratix® 10 GX/SX Device Overview Intel's 14-nm Intel® Stratix 10 GX FPGAs and SX SoCs deliver 2X the core performance and up to 70% lower power over previous generation high-performance FPGAs. Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing Stratix V Device Overview - bychips.cz Stratix V GS devices have an abundance of variable precision DSP blocks, supporting up to 3,926 18x18 or 1,963 27x27 multipliers. In addition, Stratix V GS devices offer integrated transceivers with 14.1-Gbps data rate capability. These transceivers also support backplane and optical interface applications. These Volume 2, Stratix V Device Datasheet - Chiphome Industrial devices are offered in -2, -3 and -4 core speed grades. Stratix V E devices are offered based on core speed grades while Stratix V GX, GS, and GT devices are also offered in -1, -2, and -3 transceiver speed grades. Table 1 lists the industrial and commercial speed grades for the Stratix V GX and Stratix V GS devices. Table 1. Stratix IV Device Handbook, Volume 1 - Digi-Key 101 Innovation Drive San Jose, CA 95134 www.altera.com Stratix IV Device Handbook Volume 1 SIV5V1-4.0 Design Example - 10GBase-R (Stratix V GX) - Altera Wiki Altera Transceiver PHY IP Core User Guide (PDF) - This document describes configuration details for the 10GBase-R PHY IP (Useful when generating the IP from the MegaWizard) Altera Stratix V Device Documentation - Transceiver Architecture, Clocking, Configurations and reset controller information.

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